

ABOUT THE ACS9521

This is the datasheet for the DPSync ASSP ACS9521 variant. The datasheet should be read in conjunction with the ACS9521 user guide, API documentation and other information available at the DPSync Resource Center¹.

There are many applications in which it is necessary to lock a remote clock signal to a central frequency source, and there are other applications which require the alignment of a clock to a central source of time. The ACS9521 uses DPSync packet timing technology to support both applications.

DPSync technology combines the IEEE 1588 v2 protocol with DAPU's patented packet delay filtering algorithms, which allow a reference clock to be transported across a packet switched network without special adaptations of switches or routers in the network. It is ideal for carrying timing across a legacy packet switched network. IEEE 1588 is often known as precision time protocol (PTP), the acronym that is generally used in this document.

The ACS9521 supports:

Timebase derived from:

PTP slave, SONET/SDH recovered clock, BITS/SSU input, SyncE recovered clock, GPS, 1PPS, precision holdover.

Technology bridging:

Derive timing from one input technology (SONET, SDH, SyncE, PTP) and provide timing to all outputs simultaneously.

PTP Grandmaster:

PTP Grandmaster function supports multiple PTP slaves using multicast or unicast messaging. Timebase may be PTP or ARB.

PTP Slave:

Acting as a PTP Ordinary Clock in Slave mode, the ACS9521 can lock to BCs or TCs, or it can use sophisticated packet delay filters and adaptation algorithms to lock to a remote PTP Grandmaster over a multi-hop legacy network which has no PTP support.

Self test - the device self-checks for consistency and makes rudimentary checks of the external Ethernet PHYs.

FEATURES

PTP timing features

- PTP Grandmaster selection - automatic or manual PTP master/slave mode selection.
- Powerful network delay analysis - full time-alignment in the slave over hostile networks (Layer 2 or Layer 3 networks).
- Dynamic adaptation - to network delay variations. Network loading change tolerant (e.g., ramps and steps).
- Time alignment - better than $\pm 1 \mu\text{s}$ on a managed 10-switch GbE network under G.8261²⁰ test conditions.*
- Frequency alignment - better than ± 10 ppb on a managed 10-switch GbE network under G.8261²⁰ test conditions.*

Device features

- Fully integrated - integrates hardware precision timestamping with on-the-fly insertion. Powerful integrated processor and clock recovery algorithm for PTP.
- Timing synchronization on a chip - supporting transitions from legacy circuit networks to new packet technology.
- Suitable applications - IEEE1588¹³ PTP,
- Clocks - 8 input clocks and 4 output clocks.
- Precision holdover - in all modes.
- Ports - 2 x SGMII, serial interface and JTAG.
- Time-of-day - PPS top-of-second signal plus current-time-since-epoch message on a UART.
- Output characteristics:
 - Time-aligned output pair:*
1 PPS and 125 MHz divided by n (n = 4 to 125000).
 - Frequency-aligned outputs:*
1 Hz and programmable frequency 1 kHz to 62.5 MHz.
 - Low jitter frequency-aligned outputs:*
Local oscillator: ± 20 ppm or better.
- LPGA package: 324 pin, 19 mm x 19 mm.
Lead-free - RoHS²⁶ and WEEE²⁷ compliant.
- External RAM not required.

A simplified system diagram is shown in [Figure 1](#).

* This is an indication of DAPU tested performance and is not guaranteed across all types of switches and network conditions. Please contact DAPU DPSync support for further details.

System diagram

Clock reference sources

UTC time reference (ToD info + 1 PPS clock)

GPS (ToD info + 1 PPS clock)

ARB (ToD info + 1 Hz clock)

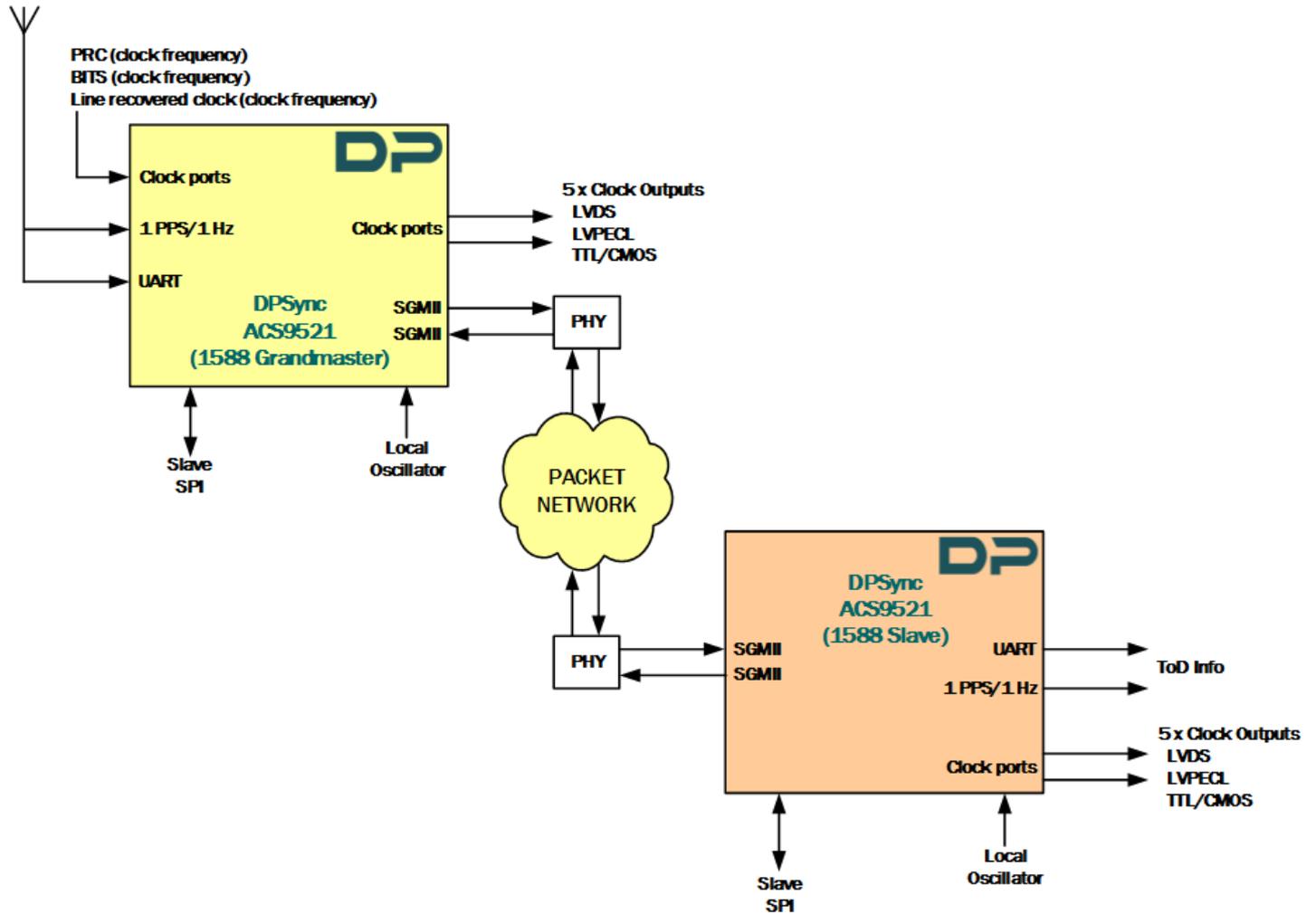


Figure 1 - Simplified system diagram - ACS9521 DPSync in PTP Grandmaster and Slave modes