

## ABOUT THE ACS9522

This is the datasheet for the DPSync ASSP ACS9522 variant. The datasheet should be read in conjunction with the ACS9522 user guide, API documentation and other information available at the DPSync Resource Center<sup>1</sup>.

There are many applications in which it is necessary to lock a remote clock signal to a central frequency source, and there are other applications which require the alignment of a clock to a central source of time. The ACS9522 combines DAPU's synchronous equipment timing source (SETS) functionality and DPSync packet timing technology and can therefore be used for both applications.

In this datasheet, the words SETS and TDM Block are synonymous, and both terms are used.

SETS functionality is used for frequency-locking applications in SDH/SONET and Ethernet equipment. DPSync technology combines the IEEE 1588 v2 protocol with DAPU's patented packet delay filtering algorithms, which allow a reference clock to be transported across a packet switched network without special adaptations of switches or routers in the network. It is ideal for carrying timing across a legacy packet switched network. IEEE 1588 is often known as precision time protocol (PTP), the acronym that is generally used in this document.

The ACS9522 supports:

Timebase derived from:

PTP slave, SONET/SDH recovered clock, BITS/SSU input, SyncE recovered clock, GPS, 1PPS, precision holdover. Physical layer clock sources are jitter and wander attenuated according to G.812, G.813, G.8261, G.8262, GR-1244-CORE, GR253 etc.

Technology bridging:

Derive timing from one input technology (SONET, SDH, SyncE, PTP) and provide timing to all output technologies simultaneously.

PTP Grandmaster:

PTP Grandmaster function supports multiple PTP slaves using multicast or unicast messaging. Timebase may be PTP or ARB.

PTP Slave:

Acting as a PTP Ordinary Clock in Slave mode, the ACS9522 can lock to BCs or TCs, or it can use sophisticated packet delay filters and adaptation algorithms to lock to a remote PTP Grandmaster over a multi-hop legacy network which has no PTP support.

TDM/clocks:

Includes all DAPU SETS family functions for physical layer input and output synchronization.

SyncE:

Integrates DAPU eSETS technology for the physical layer input and output synchronization of Ethernet PHY devices.

Self test - the device self-checks for consistency and makes rudimentary checks of the external Ethernet PHYs.

## FEATURES

### PTP timing features

- PTP Grandmaster selection - automatic or manual PTP master/slave mode selection.
- Powerful network delay analysis - full time-alignment in the slave over hostile networks (Layer 2 or Layer 3 networks).
- Dynamic adaptation - to network delay variations. Network loading change tolerant (e.g., ramps and steps).
- Time alignment - better than  $\pm 1 \mu\text{s}$  on a managed 10-switch GbE network under G.8261<sup>20</sup> test conditions.\*
- Frequency alignment - better than  $\pm 10 \text{ ppb}$  on a managed 10-switch GbE network under G.8261<sup>20</sup> test conditions.\*

### TDM timing features

- Programmable TDM timing bandwidth - for wander and jitter tracking/attenuation, 0.1 Hz to 70 Hz in 10 steps.
- Automatic hit-less source switchover - on loss of input.
- Output clock phase adjustment - in 6 ps steps to  $\pm 200 \text{ ns}$ .

### Device features

- Fully integrated - integrates hardware precision timestamping with on-the-fly insertion. Powerful integrated processor and clock recovery algorithm for PTP.
- Timing synchronization on a chip - supporting transitions from legacy circuit networks to new packet technology.
- Suitable applications - Stratum 3, 3E, 4E, 4, SONET Minimum Clock (SMC) or SONET/SDH Equipment Clock (SEC) or Ethernet, IEEE1588<sup>13</sup> PTP, Synchronous Ethernet, Ethernet Equipment Clock.
- Clocks - 18 clock inputs and 11 clock outputs.
- Precision holdover - in all modes.
- Ports - 2 x SGMII, serial interface and JTAG.
- Time-of-day - PPnS top-of-second signal plus current-time-since-epoch message on a UART.
- Output characteristics:
  - Time-aligned output pair:*  
1 PPS and 125 MHz divided by n (n = 4 to 125000).
  - Frequency-aligned outputs:*  
1 Hz and programmable frequency 1 kHz to 62.5 MHz.
  - Low jitter frequency-aligned outputs:*  
SONET and SDH OC-n rates: 3.84 MHz to 155.52 MHz.  
SyncE rates: 25 MHz, 50 MHz, 62.5 MHz and 125 MHz.
- Local oscillator:  $\pm 20 \text{ ppm}$  or better.
- LBGA package: 324 pin, 19 mm x 19 mm.  
Lead-free - RoHS<sup>26</sup> and WEEE<sup>27</sup> compliant.
- External RAM not required.

A simplified system diagram is shown in [Figure 1](#).

\* This is an indication of DAPU tested performance and is not guaranteed across all types of switches and network conditions. Please contact DAPU DPSync support for further details.

## System diagram

Clock reference sources

UTC time reference (ToD info + 1 PPS clock)

GPS (ToD info + 1 PPS clock)

ARB (ToD info + 1 Hz clock)

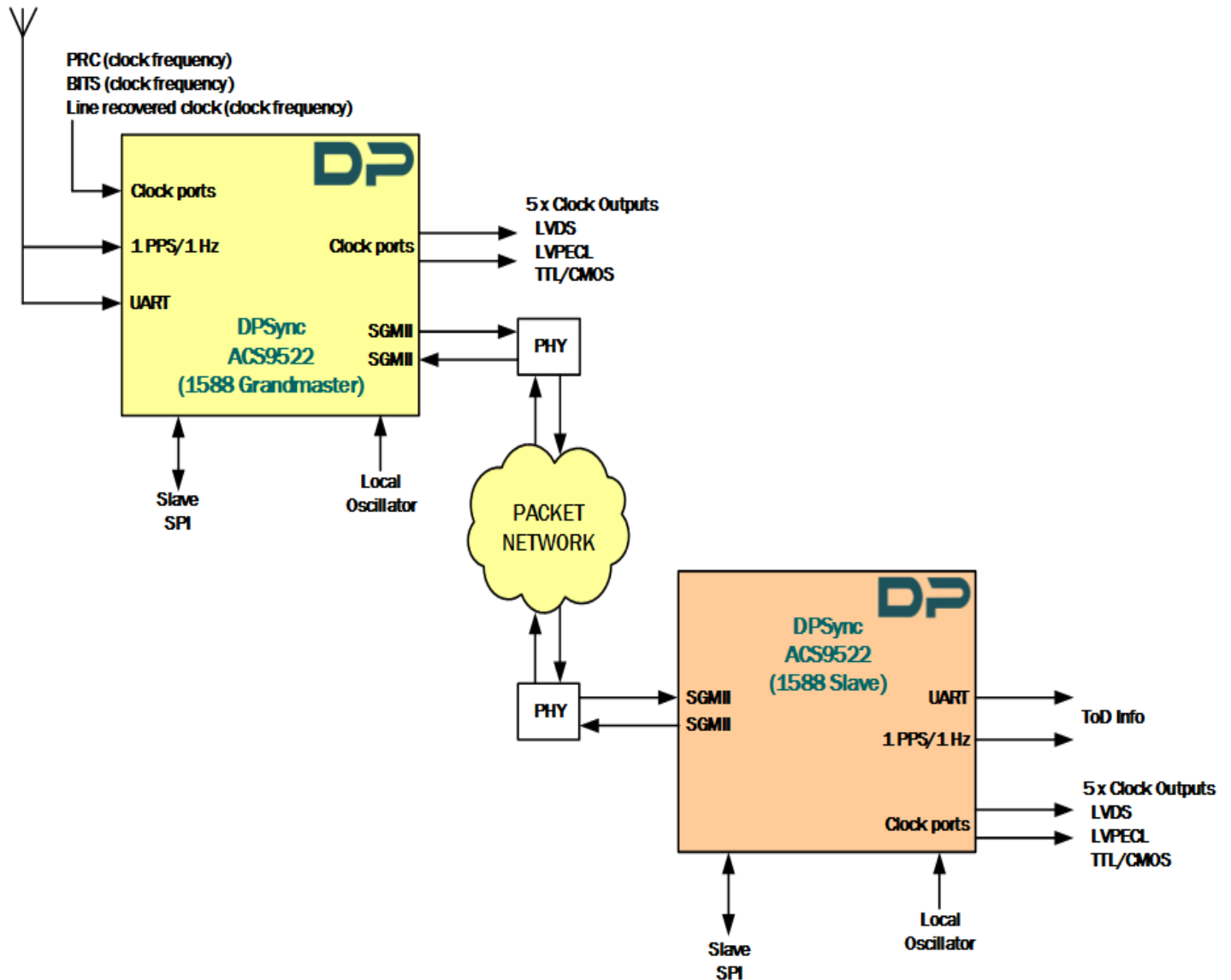


Figure 1 - Simplified system diagram - ACS9522 DPSync in PTP Grandmaster and Slave modes