## ABOUT THE ACS9528

This is the datasheet for the DPSync ASSP ACS9528.

The ACS9528 is a fully-integrated, single-chip, IEEE 1588-2008 (Precision Time Protocol) master. With the addition of an external oscillator and a time-of-day source, such as a GPS receiver, a full-featured PTP master can be implemented.

The datasheet should be read in conjunction with the ACS9528 user guide, API documentation and other information available at the DPSync Resource Center[1].

The ACS9528 features two separate PTP master blocks, driven from a common timebase, and two independent SGMII Ethernet ports. Each master block can be associated with either SGMII port for maximum flexibility. The master blocks can be individually configured to support different operating parameters of PTP, such as layer 2 (Ethernet) or layer 3 (UDP/IP), different PTP domains and one or two-step operation. Each SGMII port has individually programmable Ethernet MAC and IP addresses. By associating both master blocks to a single SGMII port, both layer 2 and layer 3 master functionality can be provided on one port.

To maximize precision and eliminate delay variation internal to the system. support for external timestamping is provided. This takes advantage of the timestamping capability built into many newer Ethernet phys and switches to allow packet ingress and egress timestamping to occur as close to the edge of the system as possible.

As well as synchronizing internal operation, the local reference oscillator can be used to provide a holdover capability in the event of the external references failing. The holdover performance is determined directly by the stability of the local oscillator, which will typically need to be a temperature-compensated or oven-controlled part if holdover capability is required.

Control of the ACS9528 can be performed over an SPI port, or the provided Windows-based GUI can be used in conjunction with the configurable plug-and-play mode to allow autonomous operation directly from reset. Since the ACS9528 contains a powerful in-built CPU complete with RAM and Flash memory, no real-time external CPU power is needed for normal operation.

## FEATURES

- Part of DAPU's market-leading DPSync device family
- Field-proven performance
- Complete dual IEEE1588-2008 master function in a single device
- Ideal for applications such as:

  PTP grandmaster
  xPON ONU
  Wireless backhaul aggregator
- Suitable for delivery of time-of-day or frequency
- 1PPS and NMEA serial port for interfacing to common GPS receivers
- Dual frequency inputs up to 160 MHz for received Synchronous Ethernet clock
- Can be used as reference for frequency-only delivery or to provide holdover stability
- Layer 2 or layer 3 operation
- Simultaneous multicast and unicast operation
- One or two-step PTP Sync messages
- Operates at up to 128 packets per second
- Supports up to 1024 slave devices

  1024 at 8 pkts/sec
  512 at 16 pkts/sec
  256 at 8pkts/sec
- Acceptable slave table (Restricts operation to known slaves)
- Support for external timestamping
- SPI interface for control
- Dual SGMII Ethernet interfaces
- DAPU-provided Windows GUI ( Can ease initial bring-up effort and reduce time-to-market ).
- Configurable plug-and-play option allows autonomous operation from reset
- Works with 10, 12.8 or 20 MHz local oscillator
- Master $I^2C$ port to control companion ACS1790 (For Synchronous Ethernet clocking)
- 324 ball, 19 x 19 mm, 1 mm pitch LBGA
- 3.3V and 1.2V power supplies
- Power consumption less than 0.5W typical
- Operating temperature – -40°C to +85°C
- Fully RoHS (6 of 6) and WEEE compliant


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# System diagram

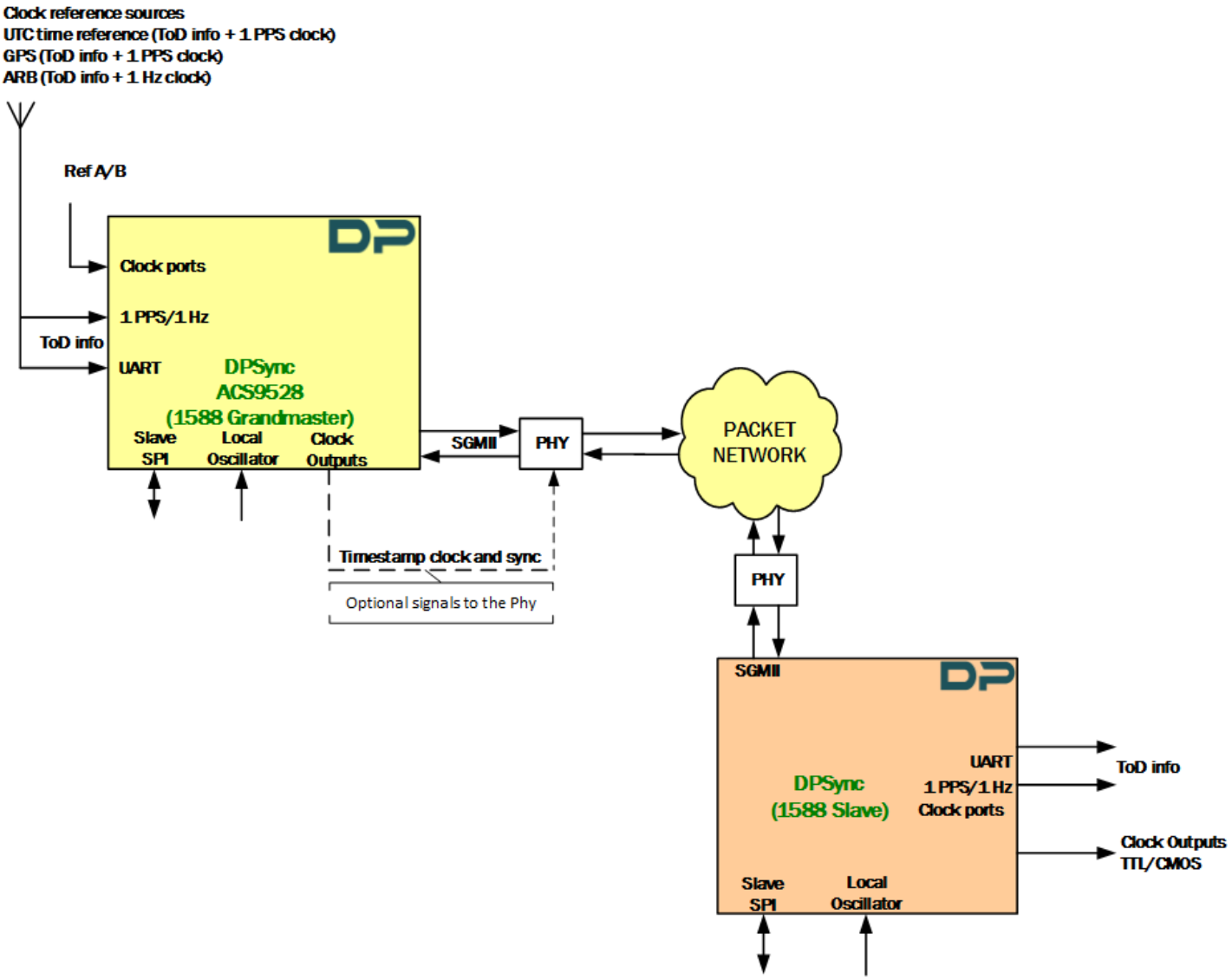


*Figure 1 - Simplified system diagram - ACS9528 Grandmaster and DPSync Slave*


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